

W. M. Long
8/14/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Keith Glidewell

Serial No.: 09/677,120

Group Art Unit: 2183

Filed: 09/29/2000

Examiner: Unassigned

For: Apparatus and Method for Process Dispatching Between
Individual Processors of a Multi-Processor SystemThe Honorable Assistant Commissioner
for Patents and Trademarks
Washington, D.C. 20231

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Technology Center 2100

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application as follows:

In the Specifications

Page 5, line 15, change "Brief Description of the Invention" to Brief Description of

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the Drawings--.

Remarks

The above preliminary amendment is being made to merely correct a minor error in a heading in the above-identified application, which is self-explanatory. The change does not introduce any issues of substance and should be entered.

If the Examiner has any questions concerning the amendment, he is courteously requested to telephone the undersigned at the number listed below.

Respectfully submitted,

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Karyn Gamm, Assistant

the processors are configured such that they can poach a process from a non-idle processor when the duration of time during which the non-idle processor is running exceeds a predetermined amount.

In a more specific aspect, the system is configured for allowing an idle processor connected electrically closest to a non-idle processor to have priority in poaching a process in the event there are more than one non-idle processors. The system is further configured to allow the time period during which a processor is allowed to remain non-idle, determined in accordance with the proximity in electrical connection between the non-idle processor and an idle processor, in which the greater the connection distance, the greater the predetermined amount of time allowed.

Other features of the invention will be understood by those of ordinary skill in the art after referring to the detailed description of the preferred embodiment and drawings.

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BRIEF DESCRIPTION OF THE INVENTION

Fig. 1 is an overview of a multi-processor data processing system.

Fig. 2A-2E shows the flow of how a process is stolen or poached by an idle processor when the processor on which it is scheduled on the queue is too busy to run the process.

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Fig. 3 shows the flow of how the job processes and relatives table is allocated such that the shortest relative time out for a job process is arranged at the top of the table, and showing how time periods are set in accordance with differences in distances between processors.

DESCRIPTION OF THE PREFERRED EMBODIMENT

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1. System Overview

Referring to Fig. 1, an overview of a multi-processing data processing system 150 is depicted. For clarity and ease of presentation, an eight-processor